

Notice of References Cited

Application/Control No.

O9/975,840

Examiner

Belur V Keshavan

Applicant(s)/Patent Under
Reexamination
CHIANG, MIN-HSIUNG

Art Unit
Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-6,146,941	11-2000	Huang et al.	438/253
	В	US-6,096,597	08-2000	Tsu et al.	438/240
	С	US-6,078,492	06-2000	Huang et al.	361/301.4
	D	US-			
	Е	US-			
	F	US-			
	G	US-			
	н	US-			
	Ι	US-			
	J	US-			
	κ	US-			
	L	US-			
	М	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	0					
	Р					
	Q					
	R					
	s					
	Т				400	

NON-PATENT DOCUMENTS

	NON-I ATEN BOCOMENTO						
*	<u></u>	Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)					
	U	S. Wolf, Silicon Processing For The VLSI ERA Volume II, PP 144-152. Lattice Press, 1995					
	٧						
	w						
	x						

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office PTO-892 (Rev. 01-2001)